REMARKS

Claims 38, 39, 42 and 43 have been amended.

The Examiner has rejected applicants' claims 38-43 under 35 USC §112, first paragraph as failing to comply with the enablement requirement. In this regard, the Examiner has argued that the specification does not describe "a converter that converts the third digital information data to fourth digital information data by combining the third digital information data, wherein the third digital information data obtained by encoding first digital information data by an encoder as being recited in claims 38 and 43." The Examiner has further argued that the specification does not describe "that fourth digital is inputted with an amount less than the first digital information for a predetermined period of time as recited in claim 42."

In order to avoid this rejection, applicants have amended applicants' claims 38, 39, 42 and 43, as above set forth. More particularly, applicants have amended applicants' claim 38 to recite a first encoder arranged to output parallel data of L bits, a second encoder, arranged to encode the second digital information data and output parallel data of M bits, where $L \neq M$, a first converter, arranged to convert the parallel data of L bits generated by the first encoder into first parallel data of N bits, where $L \neq N$, and a second converter, arranged to convert the parallel data of M bits generated by the second encoder into second parallel data of N bits, where $M \neq N$. Applicants' have amended applicants' method claim 43 similarly to amended claim 38 and have further amended applicants' claim 42 to recite that it is the second digital information data being inputted in an amount less than the first digital information data.

The above features of applicants' amended claims are clearly supported applicants'

specification at Page 15, lines 2-16, Page 31, lines 1-6 and Page 20, lines 2-21, and are shown in FIG. 12 of the applicants' Drawings. Specifically, applicants' specification discloses a first encoder (compressor 14) which encodes first digital information data by compressing the digital luminance signal output from the A/D converter 12 and outputs parallel data of L bits by supplying the compressed luminance signal data to a memory circuit 16. Page 15, lines 2-16. Applicants' specification also discloses a first converter (memory circuit 16), which converts parallel data of L bits generated by the first encoder into first parallel data of N bits by converting two 4-bit data into one 8-bit data. Page 15, lines 16-20. Applicants' specification further describes a second encoder (compressor 15) and a second converter (conversion circuit 17), where the compressor 15 encodes the second digital information data and outputs parallel data of M bits by converting an 8-bit digital MUSE signal into 6-bit parallel data, and the conversion circuit 17 then converts the parallel data of M bits into second parallel data of N bits by converting the 6-bit digital signal into 8-bit parallel data. Page 31, lines 1-16. Finally, the features of applicants' claim 42, i.e., the second digital information data being inputted in an amount less than the first information data, are disclosed on pages 14 and 31 of applicants' specification, which disclose that the frequency of the first digital information data is 44.55 MHz (Page 14, lines 23-25) and the frequency of the second digital information data is 29.7 MHz (Page 31, lines 19-20).

In summary, therefore, applicants' claims, as amended, are supported by an enabling disclosure. Accordingly, such claims are now in compliance with the provisions of 35 USC §112, first paragraph.

The Examiner has further rejected applicants' claims 38 and 41-43 under 35 U.S.C. §102(e) as being anticipated by the Enari, et al. (US 4,862,292) patent. Additionally, the Examiner has rejected applicants' claims 38-43 under 35 U.S.C. §102(b) as being anticipated by the Takahashi, et al. (US 4,513,327) patent. Claim 39 has been rejected under 35 USC § 103(a) based on the Enari, et al. or Takahashi, et al. patent taken in view of the Coleman, Jr. patent. Finally, claim 40 has also been rejected under 35 USC § 103(a) based on the Enari, et al. or Takahashi, et al. patent taken in view of the Yoshimura, et al. patent. With respect to applicants' claims, as amended, these rejections are respectfully traversed.

As previously set forth above, applicants' independent apparatus and method claims 38 and 43 have been amended to better define applicants' invention. More particularly, these claims require selectively inputting first digital information data and second digital information data, the first digital information data being different from the second digital information data. They also require first encoding the first digital information data and outputting parallel data of L bits and second encoding the second digital information data and outputting parallel data of M bits. They additionally require first converting the parallel data of L bits into first parallel data of N bits and second converting the parallel data of M bits into second parallel data of N bits. Finally, they require error correction by selectively adding an error correction check code to the first parallel data and the second parallel data, the error correction performing a common addition processing irrespectively of the first parallel data and the second parallel data.

Such a construction is not taught or suggested by the cited art of record. More particularly, the Enari, et al. patent discloses a system which operates in three modes, i.e., a

standard mode, a long playing mode and a two channel input recording mode. In the standard mode, an analog video signal is input at a terminal 10A and then passed through an A/D converter 12A, a sub-sampling circuit 14A, a distribution circuit 24 and error correction encoding circuits 26A, 26B. In the long term playing mode, a video signal also enters the terminal 10A and passes through the A/D converter 10A and sub-sampling circuit 12A. However, before being coupled through the distribution circuit 24 and the error correction encoding circuits 26A, 26B, the video signal is passed through a S/I encoding circuit 16A, which performs a block encoding action, and a time base conversion circuit 18A.

Finally, in the two-channel input recording mode, one video signal follows the same path as in the long term playing mode through to the time base conversion circuit 18A. A second video signal is received at an input terminal 10B and is processed by a sub-sampling circuit 14B, a S/I encoding circuit 16B, which performs block encoding action, and a time base conversion circuit 18B. The processed video signals from the conversion circuits 18A and 18B are then supplied to a composition circuit 20, which is arranged to combine the two video signals into a composite signal which has the same data rate as in the case of the standard mode, and the composite signal is then passed through the distribution circuit 24 and error correction encoding circuits 26A, 26B.

In the Enari, et al. patent, therefore, the input signals at the terminals 10A and 10B are all the same type of signals, i.e., analog video signals. Moreover, the S/I circuits 16A and 16B perform a block encoding action. There is, therefore, no teaching or suggestion of selectively inputting first digital information data and second digital information data, the first digital

information data being different from the second digital information data. Furthermore, there is no teaching or suggestion of first encoding the first digital information data and outputting parallel data of L bits and second encoding the second digital information data and outputting parallel data of M bits, such that L≠N. Finally, there is no teaching or suggestion of first converting the parallel data of L bits into first parallel data of N bits and second converting the parallel data of M bits into second parallel data of N bits, where L≠N and M≠N, and error correction by selectively adding an error correction check code to the first parallel data and the second parallel data, the error correction performing a common addition processing irrespectively of the first parallel data and the second parallel data.

Applicants amended independent claims 38 and 43, and their respective dependent claims, all of which recite such features, thus patentably distinguish over the Enari, et al. patent.

Turning to the Takahashi, et al. patent, it discloses a first digital video signal comprising a digital luminance signal and first and second color difference signals, and a second digital video signal relating to the same color still picture information as the first digital video signal. Col. 7, lines 58-65. The Takahashi, et al. patent further discloses that the information quantity of the second digital video signal is compressed to ¼ of that of the first digital video signal. Col. 7, line 58 -Col. 8, line 1. The second digital video signal in the Takahashi, et al. patent is obtained by separating one field of video signal into a luminance signal and color difference signals, subjecting the luminance signal to digital pulse modulation to obtain a digital luminance signal with a quantization number of 7 bits, further converting the luminance signal into a digital luminance signal with a quantization number of 8 bits, subjecting the color

difference signals to digital pulse modulation to obtain two kinds of digital color difference signals with a quantization number of 7 bits and further converting the digital color difference signals into color difference signals with a quantization number of 8 bits. Col. 8, lines 6-23. The Takahashi, et al. patent also discloses an error code correction signal and an error code detection signal added to the recording signal. Col. 13, lines 31-35.

The Takahashi, et al. patent, however fails to teach or suggest inputting first digital information data and second digital information data, the first digital information data being different from the second digital information data. Furthermore, there is no teaching or suggestion of first encoding the first digital information data and outputting parallel data of L bits and second encoding the second digital information data and outputting parallel data of M bits, such that $L \neq N$. Finally, there is no teaching or suggestion of first converting the parallel data of L bits into first parallel data of N bits and second converting the parallel data of M bits into second parallel data of N bits, where $L \neq N$ and $M \neq N$, and error correction by selectively adding an error correction check code to the first parallel data and the second parallel data, the error correction performing a common addition processing irrespectively of the first parallel data and the second parallel data.

Applicants' amended independent claims 38 and 43, and their respective dependent claims, all of which recite such features, thus patentably distinguish over the Takahashi, et al. patent.

The Coleman, Jr. patent and the Yoshimura, et al. patent fail to add anything to the Enari, et al. patent or the Takahashi, et al. patent to change the above conclusions. Applicants'

amended claims thus patentably distinguish over the combination of these patents.

In view of the above, it is submitted that applicants' claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

If the Examiner believes that an interview would expedite consideration of this Amendment or of the application, a request is made that the Examiner telephone applicants' counsel at (212) 682-9640.

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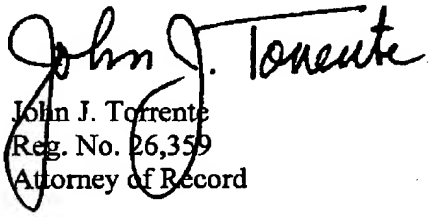
Respectfully submitted,



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